Amendments to the Specification:

Please replace the paragraph beginning at page 6, line 15, with the following rewritten paragraph:

The instruction registering stage 4 includes a ~~registration order buffer~~ Reorder Buffer (ROB) 21, an operation instruction buffer 22, and a memory access instruction buffer 23. the ROB 21 is connected to the instruction decoders 15 through decode register 18 of the instruction decoding stage 3. The ROB 21 sequentially registers all instructions in order of input and sequentially releases them in order of completion. The ROB 21 stores the order of instructions and is used to detect the dependence of on each other and to confirm the completion of instructions. The operation instructions are registered at the operation instruction buffer 22 and then issued, as will be described specifically later. The memory access instructions are registered at the memory access instruction buffer 23 and then issued, as will also be described specifically later.

Please replace the paragraph beginning at page 14, line 23, with the following rewritten paragraph:

FIG. 9 shows specific conditions of the operation instruction buffer 22 and memory access instruction buffer 23 to occur when the buffer queue control is not executed. As for the operation instruction buffer 22, when the dependence control field 68 is (logical) ONE, it shows that the operation instruction associated therewith should be issued after another instruction. The dependence control field 68 shows that the associated operation instruction may be issued when it is (logical) ZERO. The entry release field 69 shows that the associated entry may be released when it is ONE or that the entry should not be released when it is ZERO. The entry validity field 71 shows that an operation instruction is registered at the associated entry when it is ONE or that the entry is idle when it is ZERO.